CMOS Bulk Controlled Programmable Neuron for Artificial Neural Networks

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***Abstract*— In this paper, the design procedure of a novel low power neuron is discussed. Starting from the activation function circuit which is based on the modification of regulated cascode structure, a new scheme is presented which can produce the logistic function. The main advantage of the proposed function generator circuit is that its output can easily be converted to step function by means of the control voltages applied to the bulks of input stage MOS transistors. Following the concepts of the previous work by authors, the designed activation function has a good compatibility with the employed synapse. Low power and small active area consumption are the other features of the proposed circuit which qualify it for hardware implementation of neural networks. Simulation results based on TSMC 0.18µm standard process depict the correct behavior of designed circuits. The power dissipation of the activation function circuit is 60µW for 1.8 power supply voltage.**

Keywords*— *Activation Function; Artificial Neural Networks; Synapse

I. INTRODUCTION

Artificial neural networks (ANNs) constitute a family of hardware which are widely used for modeling of the central nervous systems of the animals, especially humans. They are widely used to approximate the functions which might have a large number of inputs. The schematic of Fig. 1 is used for modeling of an ANN in which any circle implies on a neural node and an arrow represents a connection between the output of a neuron and the input of the next level neuron [1].

Since 1943 where McCulloch and Pitts introduced their model of an elementary computing neuron, ANNs drew the attention of many researchers for mathematical modeling of the biological neural networks [2]. Following the developments, hardware implementation of ANNs became the topic of interest over recent years and many circuit implementations have been reported in literature to produce different models of a simple neuron [3, 4, 5, 6, 7]. In [3], the step activation function is considered as the desired membership function while in [4], [5], [6] and [7] the emphasis is on the sigmoid activation functions. Although each of the models has its own features and drawbacks, but one of the big challenges for circuit level design is the choice between voltage mode and current mode implementation [8]. One of the good methods described in [3], is the transconductance mode for synapse and transresistance mode for activation function which enables the summation of currents according to Kirchhoff's current law in the node where the outputs of all synapses are connected. It also provides the ability to apply the output voltage of the activation function directly to the synapses of the next layers and makes the implementation of multilayer neural networks possible.

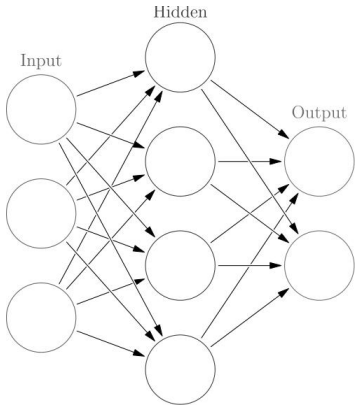

Fig. 1. A model of multilayer ANN introduced in [1].

Another challenge which could be considered in the circuit level design of an ANN, is the programmability of the neuron which increases the flexibility of the structure at the expense of the complicated system. The structures of [5] and [9] have the feature of programmability.

The other important factor for hardware implementation of a neuron is the compatibility between the synapse and activation function [5]. The simplest circuit for a synapse would be an analog multiplier. Different analog multipliers along with the comparison of their performance are completely studied in [10].

In this paper, a novel structure for activation function is presented which can generate logistic function along with step function. It utilizes a similar structure of regulated cascode circuit described in [11] with some modifications. Section II is about the design of the activation function. In section III the employed synapse circuit is briefly discussed and the compatibility between synapse and activation function is completely analyzed. Section IV contains the simulation results along with comparison of proposed architecture with previous works and finally, the conclusions are summarized in section V.

II. ACTIVATION FUNCTION

As the output stage of a neuron, the activation function has the responsibility of the decision making for the final output value of a single neuron. The most famous activation functions which are widely used in modeling of the neurons, are sigmoid functions. They have soft waveforms and their shape looks like the S letter. One of the special cases of the sigmoid function is the logistic function which is described by:

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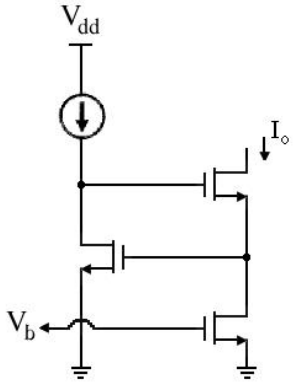

Fig. 2. Regulated cascode circuit of [11].

$$S(t) = \frac{1}{1+e^{-t}} \quad (1)$$

In this paper, the main emphasis is to produce the logistic function which has a value between 0 and 1. To do this, a modified version of the regulated cascode circuit of [11] which is shown in Fig. 2, is employed.

The modified version which is used as activation function generator is illustrated in Fig. 3. The input transistors M_1 and M_2 accept the input current from synapse circuit at the common node of their drains. For zero input current, an equal current flows in both transistors. At this point, one can say that:

$$V_{ds2} = V_{dd} - V_{gs1} \quad (2)$$

Also, for the output stage we have:

$$V_o = V_{ds3} = V_{gs2} \quad (3)$$

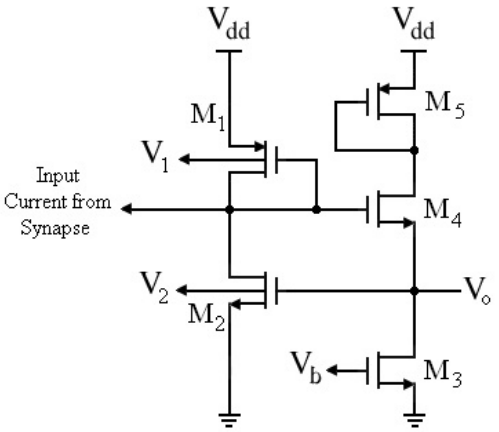

Fig. 3. Designed activation function circuit.

Applying KVL on the loop consisting of M_2 and M_4 will result in:

$$V_{ds2} = V_{gs4} + V_{gs2} \quad (4)$$

Also, for the output voltage one can say that:

$$V_o = V_{dd} - V_{gs1} - V_{gs4} \quad (5)$$

Equation (4) suggests that the gate-source voltage of M_4won't contain unexpected changes. The bias voltage of M_1 is set as for negative input currents, M_3 will operate in linear region. Therefore, the output voltage will almost be equal to zero. By applying KVL on output stage, we will obtain:

$$V_o = V_{dd} - V_{gs5} - V_{ds4} \quad (6)$$

which guaranties that the voltage drop across gate-source of M_5 will limit the upper band of output voltage to a constant value. This fact will be used as the output voltage is about to be exerted to the next layer synapse as the input.

In order to obtain the logistic function, the bulk of M_1 must be connected to the supply voltage while the bulk of M_2 is connected to the ground. For $I_{in} < 0$, the gate-source voltage of M_1 will rise and according to (5), the output voltage will remain in low level. For $I_{in} > 0$, the gate-source voltage of M_1 will start to drop. Therefore, the gate-source voltage of M_2 will rise and by means of (3), the output voltage will softly start to rise to the desired value which will be defined by (6).

In order to obtain the step function, the bulk voltages of input stage transistors must be modified. If V_1 is set to zero and V_2 is connected to the supply voltage, then the body effect of the MOS transistor increases the threshold voltages of M_1 and M_2 which makes both transistors sensitive to input current changes especially around the balance point.

Therefore, the main waveform shape controller of the circuit of Fig. 3 is the bulk voltages of the input transistors.

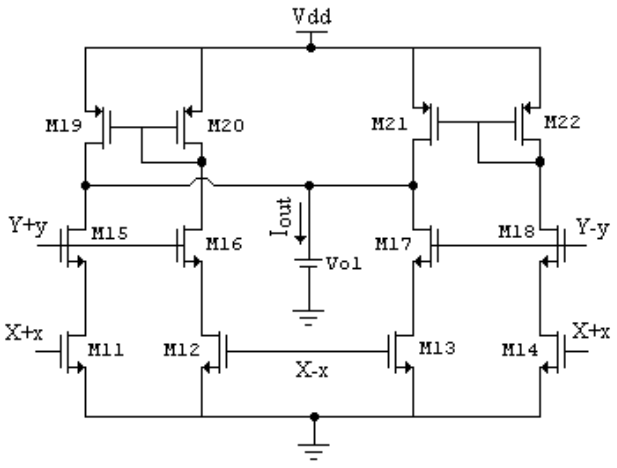

Fig. 4. Proposed synapse of [5].

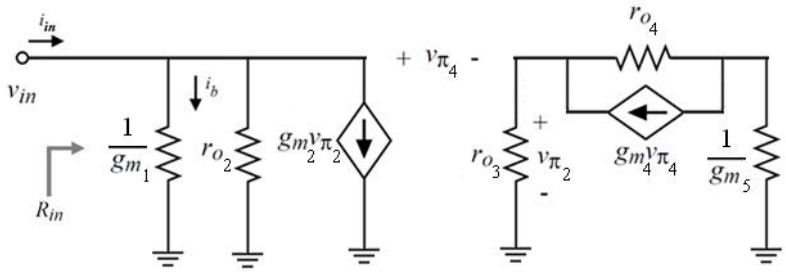

Fig. 5. Small signal equivalent ciruit for activation function circuit of Fig. 3.

III. SYNAPSE

In order to evaluate the correct behavior the whole neuron and also, to show the accuracy of activation function circuit, an appropriate synapse must be designed. By following the previous work, the proposed synapse of [5] which is shown in Fig. 4, is employed in this work to evaluate the response of the designed activation function. Therefore, it is redesignated for 0.18µm process and the voltage values are set to meet the needs between synapse output and activation function input.

But the most important section of the compatibility between the synapse and activation function is the moment in which the synapse and activation function connect to each other to constitute a neuron [5]. The output signal of the synapse is current as well as the input signal of the activation function. In order to minimize the loading effect of the activation function circuit, the input impedance of the activation function should be much smaller than output impedance of the synapse.

By using the small signal equivalent circuit of Fig. 5 for activation function, we can write:

$$R_{in} = \frac{V_{in}}{i_{in}} \tag{7}$$

By assuming that $\frac{1}{g_{m1}} \ll r_{o2}$, for the input loop, one can say that:

$$g_{m2}V_{\pi 2} = i_{in} - i_b \tag{8}$$

in which

$$i_b \cong g_{m1}V_{in} \tag{9}$$

For the output loop, we have:

$$V_{in} = V_{\pi 4} + V_{\pi 2} \tag{10}$$

The voltage drop across $\frac{1}{g_{m5}}$ will be negligible. Therefore, one can say:

$$V_{\pi 2} = g_{m4}r_{o4}\frac{r_{o4}}{r_{o3}+r_{o4}}V_{\pi 4} \tag{11}$$

which illustrates that $V_{\pi 2} \gg V_{\pi 4}$. Assuming this, simplifies (10) as:

$$V_{in} \cong V_{\pi 2} \tag{12}$$

Therefore, the input resistance of the activation function circuit will be:

$$R_{in} = \frac{1}{g_{m1}+g_{m2}} \tag{13}$$

Considering the output resistance of the synapse circuit:

$$R_{out} \cong r_o \tag{14}$$

we will observe that $R_{in} \ll R_{out}$ and the compatibility between synapse and activation function circuit is much better than that of reported in [5].

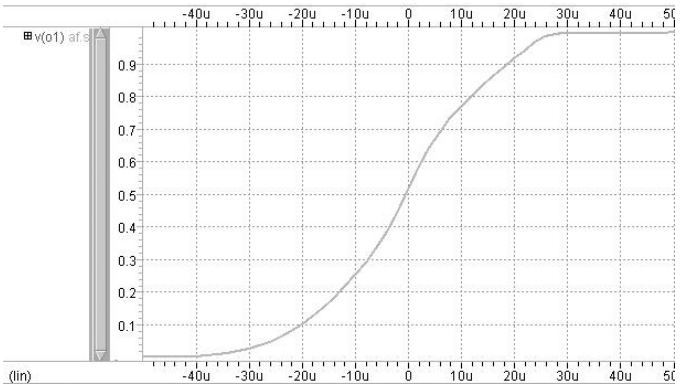

Fig. 6. Logistic output of the activation function.

IV. SIMULATIONS AND COMPARISON

Simulations are performed to the neuron circuit consisting of one synapse and one activation function as a complete neuron for TSMC 0.18µm CMOS standard process and 1.8V supply voltage. The result for logistic function is shown in Fig. 6. To explain this, one can say that the drain current of M_5 is equal to:

$$I_{d5} = \frac{1}{2}\mu c_{ox}\left(\frac{W}{L}\right)_5\left(V_{gs5} - V_{th}\right)^2\left(1 + \lambda V_{gs5}\right) \tag{15}$$

which illustrates that the current of M_5 has a cubic relation with its gate-source voltage. According to (6), (15) justifies that the output voltage will rise exponentially with input current increment. By applying the changes mentioned in section II for bulk voltages of the input transistors, the step function of Fig. 7 will be obtained.

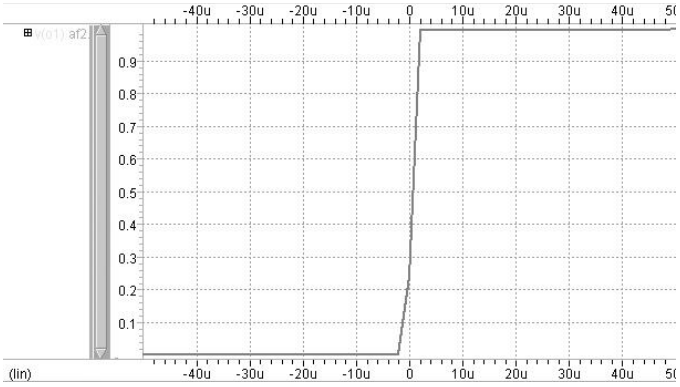

Fig. 7. Step output of the activation function.

Also, in order to show the compatibility between the synapse and activation function, the two structures are connected to each other and simulated for evaluation of the compatibility. The obtained simulation results are illustrated in Fig. 8 which confirms the compatibility feature.

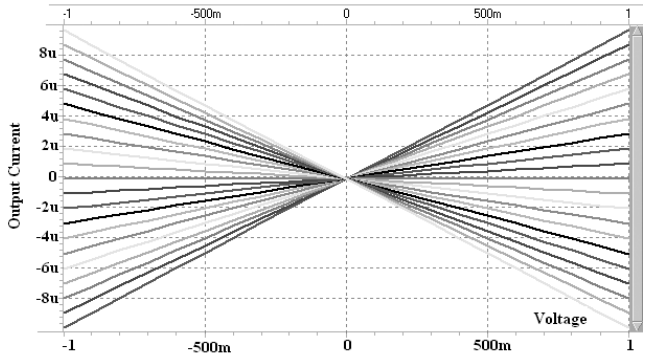

Fig. 8. The compatibility between synapse and activation function.

TABLE I. THE COMPARISON OF THIS WORK WITH PREVIOUS DESIGNS

	THIS WORK	[3]	[4]	[6]	[7]
PROCESS (µM)	0.18	0.35	0.18	0.09	0.18
LINEARITY OF SYNAPSE	HIGH	MEDIUM	GOOD	---	---
PROGAMMABILITY OF ACTIVATION FUNCTION	YES	NO	NO	NO	NO
RATIO OF AREA TO PROCESS	SMALL	LARGE	LARGE	SMALL	SMALL

The power consumption of the activation function is 60µW for the worst case of the input current. Table I shows the comparison between this work and the previous designs.

V. CONCLUSIONS

In this paper, a novel low power neuron is presented which uses small active area on chip. Starting from the activation function circuit which is based on the modification of the regulated cascode structure, a new scheme is presented which can produce both the logistic and step functions and it is the main advantage of the proposed structure. This feature is obtained by means of the control voltage applied to the bulks of the input stage MOS transistors.

Low power consumption is the other benefit of the proposed circuit which qualifies this work to be used for hardware implementation of the neural networks.

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